Analogue Ring Sampler: An ASIC for the ANTARES Telescope's front end electronic.

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ABSTRACT[1]**- The ANTARES detector is a prototype for detecting high-energy neutrinos at 1km^2 scale. It will bed on Mediterranean Sea at 2400 meters deep. It consists of a matrix of optical modules (OM) containing a photomultiplier tube. An ASIC called ARS1 has been developed to process phototube signals in order to measure their arrival time, their charge and their shape when it is different from the Single Photoelectron (SPE) one. ARS1 processes analogue signal from one optical module and converts information in digital data. All information is transmitted to the shore through readout electronic and an optical link. The paper presents the integrated circuit, front end electronic of the optical module. It integrates 24 DACs, 2 8-bit-ADCs, a 16 memory-cells pipeline to store SPE events, a complex gauge discriminator and a 4-channels 128-memory-cell 1G/s analogue sampler. The event drives the signal processing. The Pulse Shape Discriminator (PSD) identifies on line SPE pulses for which the charge and the arrival time is measured from more complex shape to be processed by the sampler. Since SPE pulses amount to 99% of the events, the dual path of signal processing provides a strong reduction of power consumption as well as of the amount of transmitted data. Each main block is explained to understand the job made by the circuit.**

1. ANTARES EXPERIMENT.

The ANTARES collaboration plans to deploy an undersea neutrinos telescope consisting of an array of optical modules. The site is located at 40km south of Toulon in France at a depth of 2400m. It allows sky coverage of 3.6π sr and 0.6π sr overlap with the AMANDA neutrino telescope. The scientific aims is to explore high energy phenomena in astrophysical object, to study topological defect in the universe, to search for neutrino produced in the annihilation processes of neutralinos captured in the center of earth, of the sun, of galaxy. (See [1]).

The ANTARES neutrinos telescope uses the detection of upward-going muons as a signature of muon neutrino interaction in the matter (The Earth) below the detector. Muons emit Cherenkov light when they go through the seawater medium. The light detected by 900 optical modules housing photomultiplier tubes (PMT) oriented at an angle of 45 degrees below the equator allows the determination of the incoming track. For this purpose, it is needed to measure the charge and the arrival time of each event detected by the PMT.

All information coming from the 10 lines consisting of 30 storeys of 3 optical modules is transmitted to the shore through a single electro-optical cable. The high number of detector channels combined with the optical link makes power consumption minimization and data compression mandatory. Adding the cost dimension, ANTARES collaboration decided to build an ASIC to respond to the detector needs.

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2. Functional description of the circuit.

II.a Introduction.

ARS1 was designed to meet ANTARES detector specification, meaning a charge measurement better than 10% and a time resolution of arrival time about the nanosecond. ARS1 is based on two others circuits ARS0 and ARS_SPE described in [2].

It is a 0.8um CMOS AMS technology circuit housing 70,000 transistors. Figure 1 shows a picture of the naked chip and its package.

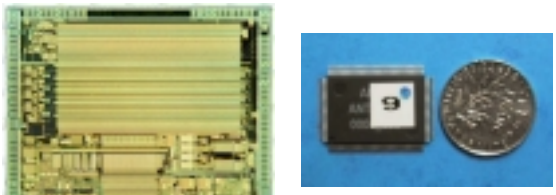


Figure 1: picture of ARS1

An ARS1 circuit is plugged to the outputs of each optical module. It records all the pulse shape coming from the PMT. Because of the detector size and the length of the optical link to the shore, electric signal cannot be transmit analogically. So ARS1 processes the analogue PMT signals and converts them in digital data.

So the circuit integrated 24 DAC for controlling parameters, two 8-bits ADC, an integrator, a time voltage converter, a 16-mixed memory-cells pipeline to store event data and a 4-channels 128-memory cells 1G/s analogue sampler.

The circuit is based on two principles: Firstly, it discriminates between single photoelectron and complex (waveform) signal. Secondly, it samples at high speed and digitised waveform pulse of up to the 4 channels, it measures charge and arrival time of single photoelectron (SPE) event. A single photoelectron event is the PMT signal when the optical module is hit by one photon. Waveform shape is the PMT signal when several photons or one photon with a higher energy hit the optical module. Since SPE pulses amount 99% of the events, the dual path of the signal processing provides a strong reduction of power consumption as well as the amount of transmitted data.

Two independent functions were added to monitor the experiment. ARS1 can send message when a too high

events rate is detected and it could send pulse train signal to an external photodiode to simulate light for the detector.

II.b ARS1 environnement.

Anode and dynode 11 of the PMT are connected to two of the 4 channels of the sampler. An anode signal, divided by ten, is connected to the third one, allowing the analysis of signal higher than 3V. The last channel samples synchronously with the anode a reference clock of 50ns needed for base of time measurement all over the detector. Anode pin is also connected to the threshold comparator, to the integrator and to the pulse shape discriminator of the ARS1.

The digital data output goes to a DAQ board for storage and transmission to the shore. As the measurement cannot bear parasitic signals, all communication signals during acquisition phase are in differential current logic with a 50µA differential level.

Because of the complexity of the design and the number of integrated components, parameters of main building block can be set via a 239 bits scan path. To study circuit behaviour, test point can be programmed in the same way than parameters setting.

To divide by two the dead times, ARS1 is able to communicate with another ARS1, increasing the sampling cells and the pipeline memory cells depth. Fast communication between each circuit is done by a token ring protocol.

II.c Functional description.

Figure 2 shows all the functionality of the circuit. ARS1 circuit is an asynchronous circuit, driven by the pulse coming from the PMT anode. When the signal crosses the triggering threshold of the comparator, a L0 trigger pulse is sent to an external L1 and L2 trigger request signals builder where coincidence between optical modules is performed. At the same time, the pulse shape discriminator block analyses the shape of signal and compares it to a predefined template and in parallel the pulse is sampled and integrated. The arrival time measurement is the amount of two data. Firstly, a time stamp (TS) value is sampled on a counter, which counts the reference clock cycle. Secondly, a time to voltage converter (TVC) block provides an analogue value proportional to the interval of time when the threshold was crossed in between two consecutive reference clock cycles. Both values are measured at the same time, when PMT signal crosses the comparator threshold.

At the end of the integration gate, depending on PMT signal charge and its duration, the PSD returns a binary result whether the pulse is of SPE or Waveform type. In both cases, this information is stored in the 16-memory-cells pipeline, as well as the pulse charge, the TVC and TS values. If the pulse is of the Waveform type, sampling keeps running for 128-samples depth before it is stopped. Signals samples are kept in memory in the fast sampling cells, outside the pipeline, waiting an eventual readout request. According to the chosen architecture, the ARS1 chip could store up to 16 SPE events but only one complex waveform pulse in the sampler. Hence, the fast sampling is no more available during the waveform event lifetime. As long as SPE events occur, it remains available.

To send out in a digital way a stored event, a L1 or L2 external trigger request signal must arrive within a predefined acceptance window associated with the event. Digitized charge, digitized TVC value, TS value and digitized samples when the event to treat is a complex shape, are sent out serially in a binary format. But, when the acceptance window ends without the occurrence of a L1 or L2 triggers, the pipeline cell associated at the acceptance window and the cells of the sampler, if it is needed, are released, waiting for a new event.

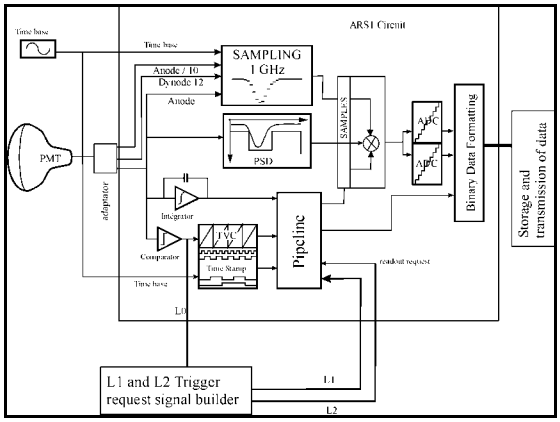


Figure 2: ARS1 architecture

Table 1 shows the performances of the circuits. As we will see, certain parameters could be adjusted with the scan path bus.

Parameters	Measured values
Power consumption	170mW (5V)
Sampler frequency	300MHz to 1.1GHz
Sampler noise (RMS)	5mV
Dynamic range of each channel	20 photoelectrons
Waveform mode gain	0.9
Integrator dynamic range	16 PhotoElectrons
Integrator transfer function	4.4mV/pC
Integrator Integral Linearity	1%
Input bandwidth	130MHz
Readout clock	10MHz to 25MHz
TVC transfer function	44.5mV/ns
TVC Noise (RMS)	800ps
TVC Integral linearity	200ps

TABLE 1: ARS1 PERFORMANCES

3. TEST BENCH OF ARS1 CHIP.

To be able to focus the most possible on the circuit performances, we automated test procedures to measure transfer functions and to control ARS1 parameters and external signals. Associated several PC data acquisition data cards with Labview software and many measurement devices increased the testability potential, the amount of

failure observation. The test bench was able to get information about the ARS1 performances and to forecast its weak point.

Basically, a FPGA controls ARS1 circuit under test operations and communication regulation with the PC. As the timing of ARS1 is around tens of nanosecond like its readout data at 20MHz, and the PC timing is around 100us to change a bit state, the Xilinx component is set via a <**command**> <**data**> protocol with the PC and put in place, after programming, different tests, and save data from the chip inside FIFO. Then, the PC comes to read each word inside the FIFO memory and analyses results.

Figure 3 shows the architecture of the test bench. Our aim was to hold invisible the hardware from a software point of view. When you build a software test, you do not want to be annoyed by hardware problem. It is what has be done, with the building of low level library where you sent <**command**> <**data**> without knowing what card is involved and what the Xilinx is doing. You read bytes from the FIFO memory without knowing what protocol is used to send them to you. Doing the test of ARS1 is just software to write.

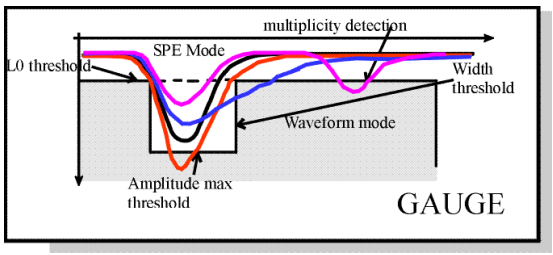


Figure 4: PSD Gauge

4. FUNCTIONAL BLOCKS OF ARS1.

In this section, we will describe main electronic blocks of ARS1 circuit in details.

IV.a. Pulse shape discriminator (PSD).

Since the SPE event has a generic shape, it is not needed to digitize such signal. We just need to measure its charge and its arrival time. Waveform pulses are unpredictable and must be fully digitized. It is the aim of the PSD to decide if the anode signal is SPE type or not. A pulse must be discriminated when its amplitude crossed a threshold named L0. Then, three criteria are used to analyze the shape on line and decide what kind of pulse it is (see Figure 4). The first gauge criterion consists of pulse amplitude. A comparator sets a threshold to a pulse level between 2 and 10 photoelectrons. The second criterion is a time over threshold criteria. The pulse width must be lower than a threshold between 10 and 50ns. The third criterion detects the multiplicity of pulse during the PSD window. All values of criteria can be set by slow control via the scan path.

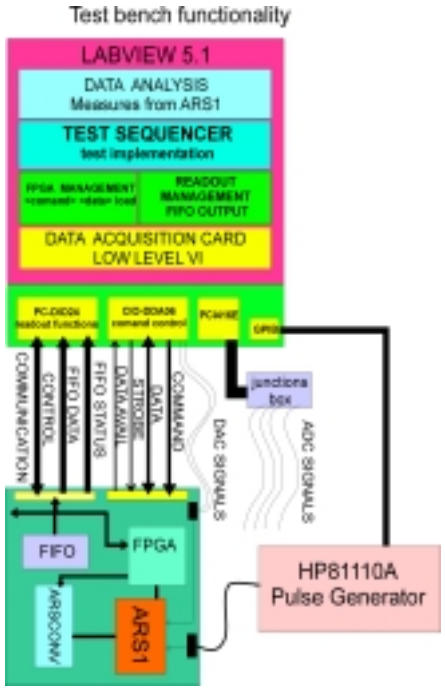


Figure 3: Test bench architecture.

The PSD is triggering by the L0 signal and gives its decision under a binary format after the integration gate ends. According to the binary result, only charge and time measurement are done for a detected SPE or the system adds digitized samples.

IV.b. Waveform mode.

Up to four channels with 128 cells could be sampled according to a frequency set between 300MHz and 1GHz. We used 1GHz for testing the chip.

The principle of the fast sampling is based on track and hold cell. [See 3]. A cell in track mode has its internal capacitor connected to the input through a switch. The capacitor voltage is following the input signal until the switch is opened, leaving the cell in hold phase, keeping in memory the input voltage (See Figure 5). The sampling frequency is defined by the delay between two consecutive commands switching off track mode to hold mode, so between 1ns and 3ns. The fast sampling is running all the time, connecting the last cell to the first cell as a ring.

When the PSD has detected a waveform event, it adds this item to the current cell of the pipeline. In the same time, the fast sampling receives a stop-erasing signal. The number of cells in hold mode increases until all the 128 cells are in hold mode, stopping the sampling and keeping in memory the input signal shape. The ARS1 has just 1ms to read and to digitize samples. The sampler is in dead time during this period.

Figure 6 and 7 shows many shapes coming from a PMT biased at 1300V and the reference clock given by the ARS1. One sees some shape saturated the chip. In this case, ARS1 records the anode signal divided by ten and also dynode 11 of the PMT. On the shore, computer can process this kind of data and gives the charge

measurement and the arrival time of the anode pulse with the match of the reference clock of 50ns.

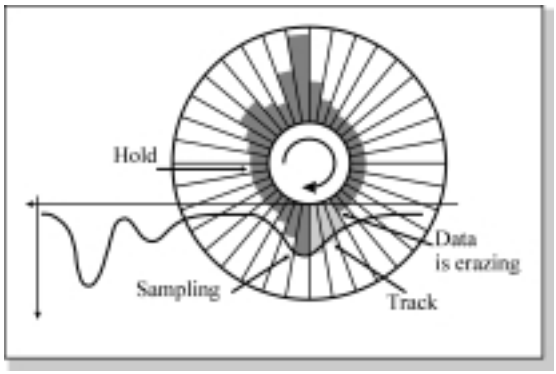


Figure 5: Ring Sampling principle

For the production test, to help for a calibration of the detector, base line slope, pedestal and noise are systematic measures and keeps in the experiment database.

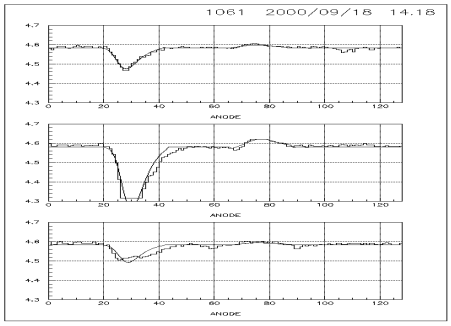


Figure 6: Examples of pulse shapes

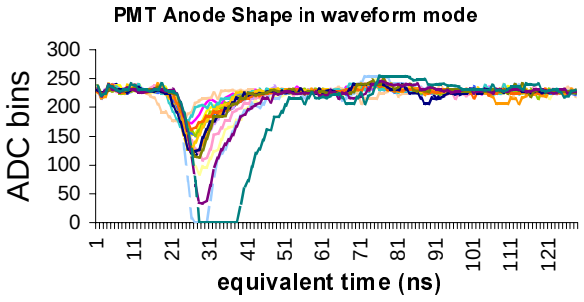


Figure 7a: Examples of anode shape

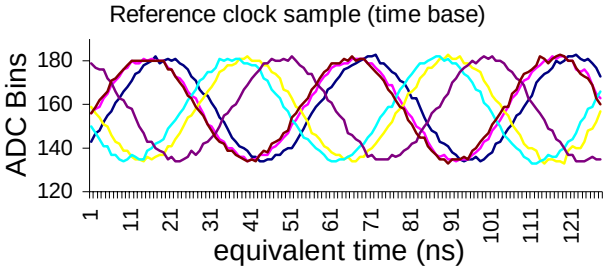


Figure 7b: Examples of reference clock

The base line of three out of four channels of the sampler has been studied. Examples are given in figure 8. Pattern noise measurement gives $3mV_{RMS}$. Measured noise, consisting of the ASIC and test bench noise, is around $5mV_{RMS}$. The base line has a slope around 20µV/ns (see figure 8) for the three channels because of the amplifier, which reads each cell. This value is stable and is saved for each circuit.

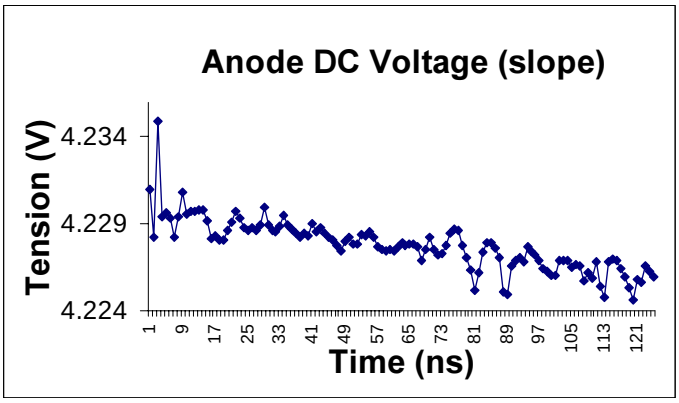


Figure 8a : Anode base line example

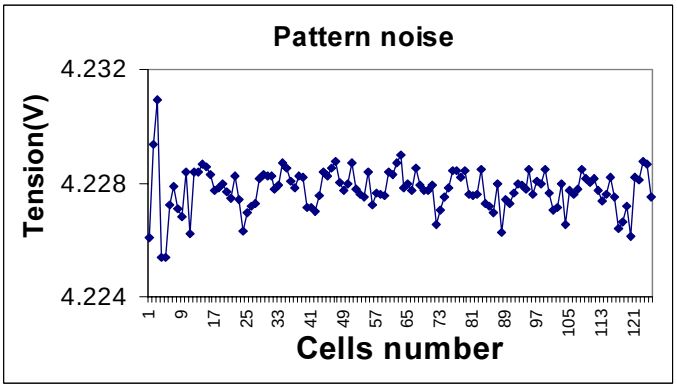


Figure 8b: Pattern noise

IV. c. SPE mode.

The SPE mode consists of measuring the charge and the arrival time prior to the reference clock of 50ns of the PMT anode pulse.

As the arrival of an anode pulse is random, and as we want to get all the charge, the integration is made by part. The complete integration gate consists of a first step before the pulse crossed the L0 threshold and a second step after this moment. ARS1 generated a clock with a predefined period, which is the integration gate for the first part. One cycle corresponds to three phases: an integration step, a memorization step and a reset step as seen in figure 9. This cycle is copied three times. Each step is applied to a switched capacitor, meaning they are one capacitor in integration, one in memorization and one in reset. At the end of the second integration part where a new integration gate width has been set, ARS1 sums the capacitor in

integration and the one in memory. This is the charge value, which will be digitized if needed.

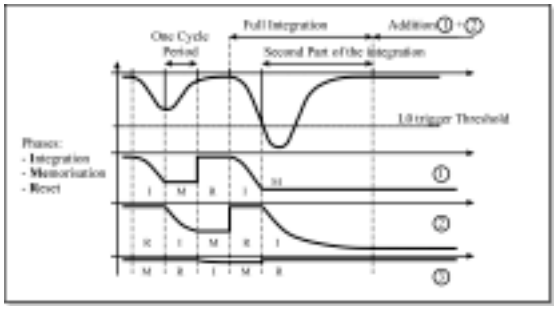


Figure 9: Integration by part.

For the experiment, the transfer function slope see in figure 10 is set to 4.5mV/pC (5% fluctuation from one ASIC to an other) to optimize the dynamic of the integrator. The relative error is about 1% compared to 10% specified. Figure 10 and 11 show the Charge transfer function for one ASIC.

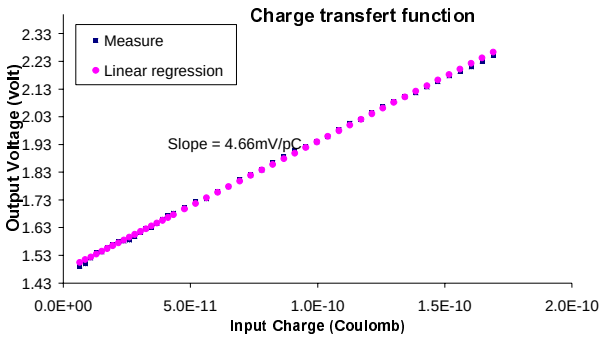


Figure 10: Examples of Charge transfer function

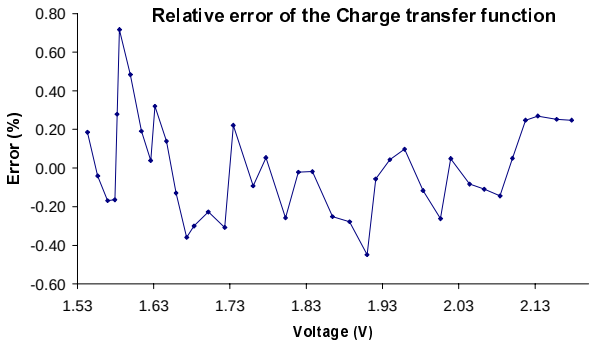


Figure 11: Example of Integral linearity error of one ARS1

The arrival time is measured in two parts: A time stamp is provided for long-term time information when the trigger L0 was crossed. It is a 24 bits counter clocked by the reference clock. The less significant bit of the counter is directly the reference clock itself in order to avoid any ambiguity in the time stamp value with respect to the Time Voltage Converter (TVC).

The TVC is a ramp generator given a voltage proportional to the reference clock period. As soon as an anode pulse crossed the L0 threshold, the ramp is frozen and memorized.

The arrival time is gotten by the Time Stamp digital value and the analogue TVC value, which will be digitized later on with one of the two internal ADC.

Figure 12 shows the transfer function of the TVC with corresponding time stamp value. One measures, in mean, a noise about 800ps with a linearity of 200ps on several ARS1. The noise is twice than expected because of external source on the test bench and power supply fluctuation. But the value remains good for the experiment.

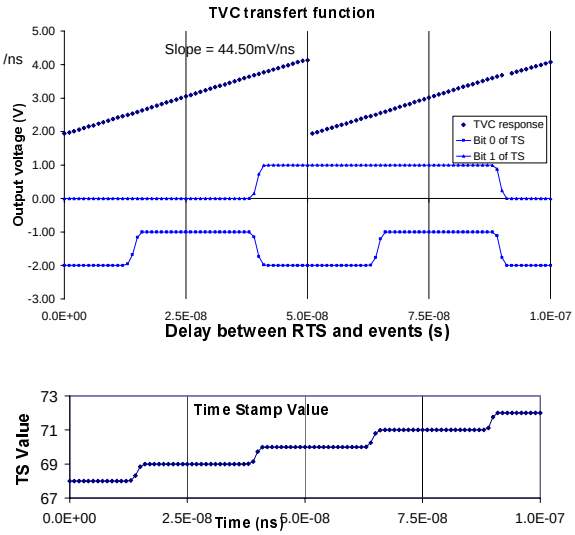


Figure 12: arrival time transfer function of an ARS1.

Practically, an external signal, called Reset Time Stamp (RTS), arrives periodically to reset the counter for giving a time start. Counting each RTS period plus the time stamp value and the TVC value give an accurate date of the event if it is SPE. Otherwise, we use the shape of the pulse with respect to the digitized reference clock.

Both values are saved in one of the pipeline cell if it is not full, waiting for a readout request.

IV.d. Mixed 16 memory cells pipeline.

The pipeline is a 16 memories consisting of analogue and digital cells to keep charge, TVC analogue values, Time Stamp value and also two others binary information. One bit indicates if the event is of waveform type and a second showing if the sampler contains the waveform shape. Indeed, when the sampler is in dead time and another waveform type is detected, it is treated as a SPE. Thus, the pipeline frees the integrator, the TVC and the Time stamp in few 100 ns, after having written data in a memory cell.

One needs to keep values until a trigger request arrived or when the waiting time is ended. Depending of the detector

size and the distance between ARS1 and L2 elaboration triggers, the acceptance window of L2 could reach several ten of microsecond. Until the pipeline is full, ARS1 manage to accept events because of this memory and decrease the dead time.

A write manager, a trigger manager and a read manager control the pipeline. The trigger manager aims is to authorize readout request during the write time. L1 readout request could come back from L0 signal only few tens of ns (near coincidence) and must be accepted during the pipeline write phase. L2 readout request must come later depending on the detector size and the distance between the L2 trigger builder and the ARS1. So the acceptance window starts after a waiting time began when the memory cell is written and could end few microseconds later. Examples of pipeline management are showed below.

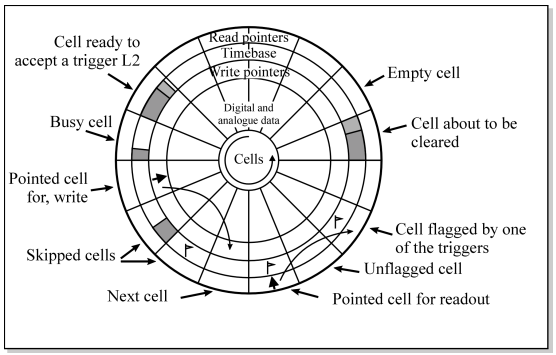


Figure 13: Examples of the pipeline management.

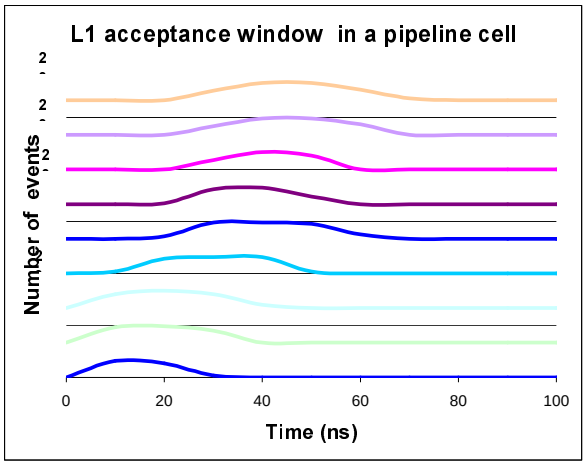
L1 and L2 acceptance window and L2 waiting time are set by slow control parameters. Figure 12 shows different acceptance window starting when the pipeline cell is written. By slow control, one could choose the width, the delay with respect to the start of writing in the cells. With that, one could adjust perfectly delay and window matching between ARS1 and the trigger builder.

IV.e. Readout data.

Other information than SPE and Waveform event could be sent to the shore for controlling the experiment. Each time a slow control data is sent, a status event is thrown to give Time Stamp value. The previous value of the Time stamp counter is sent after ARS1 received a RTS signal. ARS1 allowed the monitoring of the event rate and sent a counting rate monitor event to the shore, giving the event rate. So ARS1 manages six types of events:

1. Counting Rate Monitor event (1)
2. Waveform with the four channels because of saturation.(2)
3. Waveform with only anode and clock reference data. (2)
4. SPE event. (2)
5. Reset Time Stamp event (3)
6. Status event.(4)

Each event has a priority level for readout processing, displayed between parse. But the processing is always the same. As soon as an event is ready to be sent, the read operation consists of connecting the storage capacitor for analogue value to one of the two 8 bits ADC input.



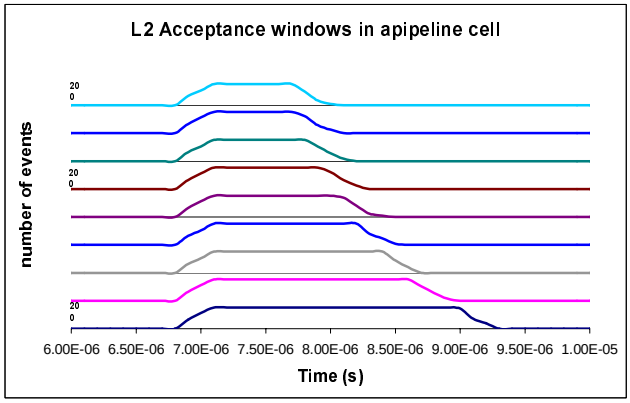


Figure 14: Example of acceptance window measurement.

Digital values are sent directly to the digital data formatter, waiting all data corresponding to the processed event.

		Bit number							
yte	Name	0	1	2	3	4	5	6	7
	Header	A0	A1	T0	T1	T2	WM	E/D	CR
	Time Stamp	LSB							LSB +7
		LSB +8							LSB +15
		LSB+ 16							LSB +23
	TVC(T)	T7	C7	T6	C6	T5	C5	T4	C4
	Charge (C)	T3	C3	T2	C2	T1	C1	T0	C0
	Waveform Adress	LSB						LSB +6	
non valid bits									
	Ref Clock (R)	R7	A7	R6	A6	R5	A5	R4	A4
	Anode (A) #0	R3	A3	R2	A2	R1	A1	R0	A0
2 non valid bits ……									
61	Ref Clock (R) Anode (A) #0	R7	A7	R6	A6	R5	A5	R4	A4
62		R3	A3	R2	A2	R1	A1	R0	A0

TABLE 2: DATA FORMAT OF THE WAVEFORM EVENT.

After digitization, all data are put in series and provided on one single output signal clocked by an external readout clock. Each event has got a common format consisting of a

header and a data body as showed on table 2 for an anode event (type 3):
For analogue data processing, ARS1 has got two identical 8-bits ADC of successive approximation type (dichotomy). As can be seen on figure 15, they consist of a digital to analogue converter whose output voltage is compared to the input voltage to convert. Conversion is clocked at 10MHz, meaning that eight pulse period are needed to reach a complete result. Each ADC has a set-up of two parameters taken among three possible values saved in register bank. One parameter defines the LSB value and the other is the maximum convertible voltage (4.87V). Slow control parameters can modify these values. With the readout sequencer, each bank corresponds to an analogue data type to convert (table 3):

ADC #1	Bank n°1 (5 bits)	Anode divided by 10 signal
	Bank n°2 (5 bits)	Anode Signal
	Bank n°3 (5 bits)	SPE Charge
ADC #2	Bank n°1 (5 bits)	Dynode 11 Signal
	Bank n°2 (5 bits)	Reference clock
	Bank n°3 (5 bits)	SPE TVC

TABLE 3: LINK BETWEEN ADC BANKS AND DATA VALUES.

Figure 16 shows example of transfer function for 4 parameters setting. It displays the full scale of the ADC (0,31), scale chosen for Charge and TVC conversion values, and the lowest scale. Corresponding data are showed in table 4.

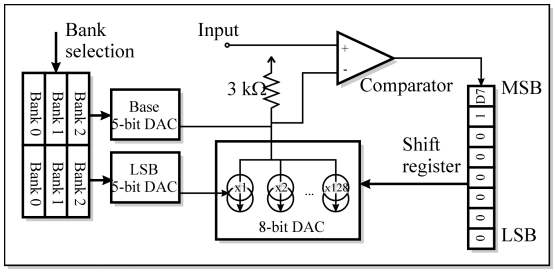


Figure 15: ADC Structure

As seen in table 4, we noticed up to 10% between parameters set and real measurement because of the fluctuation of the resistance giving the current reference of the DAC. Meanwhile, the series test of the chip allows the error measurement and allows to calibrate results for physics.
We note that in full scale (0,31), the ADC does not work correctly until it reaches 1V. The chip needs a power supply between 0 and 5V. Until the MOS threshold is not reach, amplifier inside ADC does not work linearly. The lowest configuration which is possible is not linear too because the asked current in the DAC is too small, and transistors are not working linearly, moreover, the LSB is lower than noise, this two effects give a bad behavior of the ADC for LSB under 3mV.

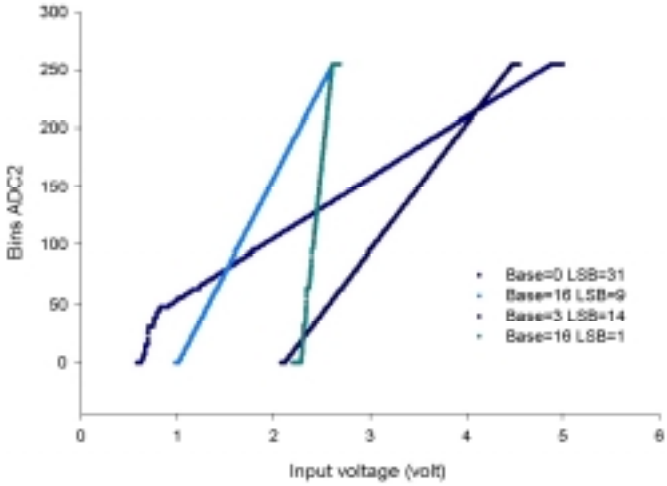


Figure 16: transfer function of 8 bits ADC for four bank of values

Banks Values	*(0,31)* (4.87V, 19.6mV)	*(16,9)* (2.87V, 5.75mV)	*(3,14)* (4.495V, 8.6mV)	*(16,1)* (2.87V, 1.19mV)
Vmin(V)	*1*	*1.01*	*2.1148*	*2.2808*
Vmax(V) Error	*4.8678* (0.2%)	*2.619* (8.74%)	*4.4782* (0.37%)	*2.6153* (8.87%)
Dynamic (V)	3.8678	*1.609*	*2.3624*	*0.3345*
LSB (mV) Error	*19.1* (2.55%)	*6.23* (7.4%)	*9.252* (7.04%)	*1.69* (42%)

TABLE 4: MEASUREMENT RESULTS FOR ONE ADC OF ONE ARS1.

IV. f. Miscellaneous Functions.

In order to limit the dead time of ARS1 during acquisition, one chains two ARS1 together as said before. The communication protocol is based on a token, which is transmitted from one ARS1 to the other, allowing the process of event. As soon as a L0 trigger signal exists, the ARS1, which has the token, is going to do the measurement and give the token to the other if the last is available for next event (not in dead time).

ARS1 is a chip, which has 75 parameters to be set for doing a good job. These 75 parameters represent 239 bits. So a slow control sequence is initiated each time it is needed to program the circuit. It is a serial protocol. On one side, a scan path throughout the circuit from one register to another constitutes the slow control architecture. Each register controls DACs. They are 24 of these DAC with 3 to 8 bits as input value. On other side, a state machine decode slow control frame coming from an external bus common to all ARS1 chips. One can write

and read slow control parameters depending on a protocol format. After that a header is decoded, ARS1 can accept data from outside or can throw away data on the same line. This line is bi-directional.
Some of this parameters add test functionality for debugging and also, disables some functions. It is the case, for example, to the L1 or L2 request. One could set a bit to trig all events without waiting for a L1 or L2 external signal. One could test the data readout machine, sending out pseudo-events to check the format of the data. There is also special pin out to display internal signal, to inject stimuli. It is programmable by slow control.

ARS1 has a LED pulse generator. This function allows trigging external photodiode, simulating light in front of PMTs. The generator provides one or 1024 pulses of at least 50ns width on the output, depending of slow control setting.

IV.g. Dead Time analysis.

The ARS1 dead time consists of three independent part. The first one is the dead time associated to the TVC and integration measurement. When an ARS1 processed an event, it cannot process a new event. This dead time depends of the integration gate, the write time in the pipeline. We evaluate it from 120ns to 500ns according to the data set by slow control. The second one is the dead time associated to the sampler. When an event is declared waveform, ARS1 stored all the samples until they are read or erased. It takes up to 60us to take the decision and 335us to sent out data for the 4 channels. The last dead time concerns the saturation of the pipeline memory. It depends on the readout clock period to withdraw cells information. One sees on the figure 17 a simulation of the dead time when we use an ARS1 without pipeline, one with pipeline and when we link two ARS1. As the event rate is around 60kHz, we need the pipeline, and with two ARS1 linked together, we are sure not to loose event.

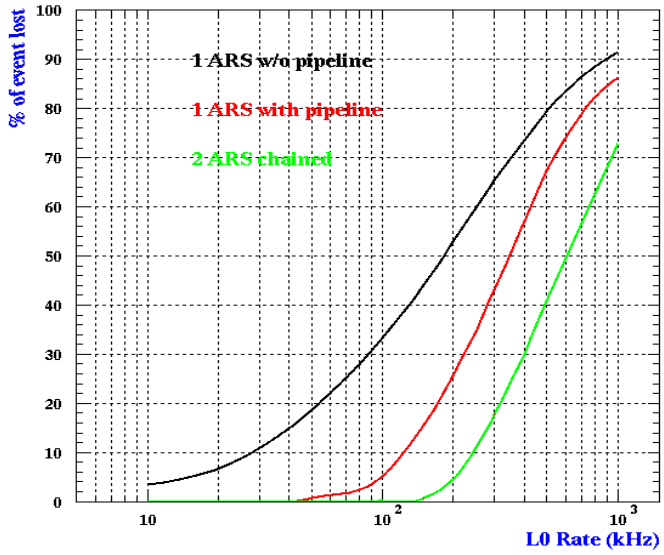


Figure 17: Simulation of event lost

5. Conclusion

ARS1 circuit has shown good results for the expected physic of Antares. The circuit is not a part of a measurements system but the system itself. It is a step to the future in microelectronic for physics. It manages to take decision on line, earning time for measuring next event. It will be used for prototyping 6 detections nodes for 2002. The complexity of the design, because of the number of electronic functions and the decision to make an asynchronous circuit was a challenge for Antares collaboration. This challenge is in way to be winning because we planned to do a production run at the beginning of 2002 year for the 0.1km^2.

Reference

[1] A deep Sea telescope for high Energy Neutrinos, **astro_ph/9907432** . *http://antares2.in2p3.fr*

[2] D. Lachartre, F. Feinstein," Application Specific Integrated Circuits for Antares Offshore Front-end Electronics", Proceeding on new developments in photodetection (NIM) Beaune june 21-25, 1999 p 99-104

[3] G. Haller and B. A. Wooley, " A 700MHz Switched Capacitor Analog Waveform Sampling Circuit", IEEE journal of solid state circuits, vol 29, n°4, April 1994 p 500-508.